Homework 2 Solutions

1) You are working on a project for your computer networks course and you are supposed to send an IP address 130.85.24.91 as a raw 32 bit number across TCP to your friend. (You use standard library functions such as ntohl and htonl in C) You are running Solaris OS on a SPARC machine while your friend is running Linux on an Intel x86 machine. How is the IP address represented in

    a. Your computer   8255185B
    b. While in the network   8255185B
    c. Your friend's computer   5B185582

    Give the values in Hexadecimal.   (15 points)

2) Assume that registers R2, R3 and R4 store initial values of 200, 300 and 400 respectively. Also assume that Mem [200] =25, Mem[300] = Mem[400] = 50, Mem[500] = 100, Mem[596] =40, Mem[600] = 200, Mem[700] = 100, Mem[1000] = 150, Mem[1200] = 300, Mem[1600] = 400 What value will be stored in register R1 and in R2 in each of the following cases:
(Assume sequential execution with no pipelining)
    a. ADD R1, R2, R3
    b. ADD R2, R4, #15
    c. ADD R1, R2, (R4)
    d. ADD R2, R3, 100(R4)
    e. ADD R1, R2, (R3+ R4)
    f. ADD R2, R4, (600)
    g. ADD R1, R2, @(600)
    h. ADD R1, R3, (R2)+ (assume d=4)
    i. ADD R1, R4, -(R2) (assume d=4)
    j. ADD R1, R2, 100(R3)[R3] (assume d=4)   (40 points)

	a	b	c	d	e	f	g	h	i	j
R1	500	500	465	465	500	500	625	500	600	1000
R2	200	415	415	400	400	600	600	604	600	600

3) We have a single stage, non-pipelined machine and a pipelined machine with 5 pipeline stages. The cycle time of the former is 5ns and the latter is 1ns.

    a. Assuming no stalls, what is the speedup of the pipelined machine over the single stage machine?

        Speed up = 5ns/1ns = 5

    b. Given the pipeline stalls 1 cycle for 40% of the instructions, what is the speed up now?

        Pipeline loses 1 cycle 40% of the time. CPI is now 1.4.

        Speed up = (1 CPI * 5ns) / (1.4 CPI * 1ns) = 3.58

                                  (10 points)

4) (C.1 from the text book "Computer Architecture, A Quantitative approach" 5th edition)

Use the following code fragment:

```
Loop:    LD        R1, 0(R2)
         DADDI     R1, R1, #1
         SD        0(R2), R1
         DADDI     R2, R2, #4
         DSUB      R4, R3, R2
         BNEZ      R4, Loop
```

Assume that the initial value of R3 is R2 + 396.

    a. List all the data dependencies in the code above. Record the register, source instruction and destination instruction; for example, there is a data dependency for register R1 from LD to DADDI.

    (Circle the two registers in the code and use an arrow to point the dependency)   (10 points)

b. Using a pipeline timing chart like Figure A.5 (4th edition) or Figure C.5 (5th edition) from the textbook, show the timing of this instruction sequence for a 5 stage pipeline along with the number of cycles required to execute one iteration of the loop with (i) No forwarding and (ii) With full forwarding. Assume registers can be written and read in the same cycle, during writeback.

(The number of cycles for the execution of one iteration of the loop ends after the EX stage of BNEZ instruction)   (20 points)

i) 16 cycles

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
LD	F	D	E	M	W												
DADDI		F	S	S	D	E	M	W									
SD				F	S	S	D	E	M	W							
DADDI							F	D	E	M	W						
DSUB								F	S	S	D	E	M	W			
BNEZ											F	S	S	D	E	M	
outside															F	S	S
LD																	F

ii) 9 cycles

	1	2	3	4	5	6	7	8	9	10	11
LD	F	D	E	M	W						
DADDI		F	S	D	E	M	W				
SD				F	D	E	M	W			
DADDI					F	D	E	M	W		
DSUB						F	D	E	M	W	
BNEZ							F	D	E	M	W
outside								F	S	S	
LD										F	

c) Assuming the branch has one delay slot, rewrite the code to fill in that slot. How many cycles does it take to execute one iteration of the loop now?

(5 points)

8 cycles

```
Loop:    LD        R1, 0(R2)

         DADDI     R1, R1, #1

         DADDI     R2, R2, #4

         DSUB      R4, R3, R2

         BNEZ      R4, Loop

         SD        -4(R2), R1
```